PATENT
Docket No.: 00484/45

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT : Kazutaka NAKA et al.

SERIAL NO. : Unassigned

FILED : February 11, 2002

FOR : VIDEO SIGNAL PROCESSING DEVICE FOR AUTOMATICALLY ADJUSTING PHASE OF SAMPLING CLOCKS

ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

PRELIMINARY AMENDMENT

SIR:

Prior to examination of the above-identified application, please amend the specification as follows.

IN THE SPECIFICATION:

Please amend the specification as follows.

Following the Title of the application, please insert the following:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of Application Serial No. 09/225,348 which was filed on January 5, 2001, which is a Continuation-in-Part of U.S. Serial No. 08/687,240 which was filed on July 25, 1996 and issued as U.S. Patent No. 5,990,968 on November 23, 1999.--

Page 1, paragraph #2:

2. Description of Related Art

Video signals which are output from an engineering work station, a personal computer or a display terminal of a computer are output as an signal based on dots which correspond to picture elements on a display screen.

Page 2, paragraph #6:

If the phase of the sampling clocks is not accurately coincident with the dot phase, picture elements frequently occur that have obscure intermediate gradation at an edge portion corresponding to a shift from white to black or from black to white, resulting in degradation in image quality. The degradation in image quality is particularly apparent when characters or fine patterns are displayed.

Page 2, paragraph #7:

In general, the frequency of the dots on the video signals (hereinafter referred to as "dot frequency") is set to an integer multiple of the horizontal scanning frequency of a display. Therefore, in the prior art, those signals which are synchronized in phase with horizontal synchronizing signals and have the frequency of the integer multiple of the horizontal scanning frequency are generated by a PLL (Phase Locked Loop) circuit, thereby generating sampling clocks which are synchronized with the phase of the dot phase of the dot frequency.

Page 2, paragraph #8:

As described above, the sampling clocks are controlled to be synchronized with the horizontal synchronizing signals by the PLL. However, actuality, the phase of the sampling clocks generated on the basis of the synchronizing signals is not always synchronized in phase with the dot phase due to the processing delay of a synchronizing separating circuit for separating the horizontal synchronizing signals from the video signals (when the synchronizing signals are transmitted while superposed on the video signals), the difference in processing delay between the horizontal synchronizing signals and the video signals which are normally processed in a different system, or the variance between the length of a transmission cable for transmitting the horizontal synchronizing signals and the length of a transmission cable for transmitting the video signals (when the synchronizing signals are transmitted independently from the video signals). Therefore, in this case, the phase of the sampling clocks or the synchronizing signals is required to be delayed through a delay line, thereby adjusting the sampling clock phase.

Page 4, paragraph #10:

Such a phase adjustment is needed every time a device for outputting the video signals and the synchronizing signals to be sampled is replaced by another, or when the horizontal scanning frequency or the dot frequency of the input video signals is varied.

Page 5, paragraph #15:

In order to attain the above object according to the present invention, the video signal processing device in which video signals representing an image are converted to multi-valued digital data representing picture elements each contained in the image at a timing based on sampling clocks, includes conversion means for successively sampling the video signals at the timing based on the sampling clocks to convert the video signals to the multi- valued digital data, classification means for successively classifying the converted multi-valued digital data into a low-level picture-element data group having values contained in a first value range and a high-level picture-element data group having values contained in a second value range which are higher than the values of the first value range, calculation means for successively calculating statistics which are based on the variance of the values of low-level picture element data in the classified low-level picture-element data group and the variance of the values of high-level picture element data in the classified high-level picture-element data group, and adjustment means for adjusting the phase of the sampling clocks on the basis of the successively calculated statistics so that the variance of the values of the low-level picture element data and the variance of the values of the high-level picture element data are reduced.

Page 6, paragraph #17:

That is, in the video signal processing device, the multi-valued digital data converted in the conversion means are classified into the low-level picture element data group having the values contained in the first value range and the high-level picture element data group having the values contained in the second value range which are higher than the values of the first value range in the classification means, and the statistic which is based on the variance of the values of the low-level picture element data in the classified low-level picture element data group and the variance of the values of the high-level picture element data in the classified high-level picture element data group is

successively calculated in the calculation means. If the sum of the variance of the values of the low-level picture element data in the low-level picture element data group and the variance of the values of the high-level picture element data in the high-level picture element data group are used as the statistics, the two variance values and the sum of the variance values are minimized when the sampling clock phase is properly adjusted because no obscure intermediate gradation occurs.

Page 7, paragraph # 23:

Fig. 5 contains graphs showing the relationship between the sampling clock phase and the occurrence frequency of (a) the data of the difference AT between the average values of white picture element data and black picture element data, and (b) the total variance VT of the variance of the white picture element data and the variance of the black picture element data;

Page 8, paragraph #24:

Fig. 6 is a block diagram showing the construction of a main part for generation of sampling clocks in a write-in control circuit according to the embodiment of the present invention;

Page 14, paragraph #46:

The details of the phase adjustment of the sampling clocks in the video processing device 18 as described above will now be described.

Page 14, paragraph #47:

The video signal generator 19 inputs, as video signals, a test pattern which comprises signals having two gradation levels, for example, a black signal (0% brightness) having a level lower than a predetermined level and a white signal (100% brightness) having a level higher than the predetermined level and in which variations from black to white and from white to black occur relatively frequently.

Page 21, paragraph # 62:

Upon an instruction to adjust the sampling clock phase from the controller 21 through the communication terminal 16 after the video signal generator 19 starts to input the input video signals

VI of the black and white pattern as shown in Fig. 4A, the MPU 9 first reads data from the memory 6 to calculate the average difference AT and the total variance VT (first). Thereafter, the phase of the sampling clocks generated in the write-in control circuit 5 on the basis of the control signal CKPH from the MPU 9 is varied in a specific direction (for example, a plus direction). In this state, the data which are sampled and digitally converted in the A/D converter 4 are read out from the memory 6 again to calculate the average difference AT and the total variance VT (second).

Page 26, paragraph # 75:

Furthermore, the processing of the MPU 9 is realized by the processing program written in the ROM 10. Accordingly, the sampling clock phase can be automatically adjusted to the optimum value with no operator's work by merely generating video signals representing a predetermined test pattern from the video signal generator 19 and giving an instruction to adjust the sampling clock phase from the controller 21 to the MPU 9.

Page 27, paragraph # 78:

Furthermore, the MPU 9, the ROM 10 and the RAM 11 are constructed as independent and separate elements in Fig. 2. However, these elements may be designed in a one chip microcomputer so that the ROM or RAM is built into the MPU.

Page 28, paragraph # 81:

The MPU 9 can obtain data of any position on the screen from the memory 6 insofar as the position is within an area which comprises white picture elements and the black picture elements and represents a pattern having a variation from white to black or black to white. For example, a sampling miss occurring at the center portion of the screen at which deterioration is liable to be noticeable can be sufficiently suppressed by optimizing the sampling clock phase with the data corresponding to the picture elements in an area at the center portion of the screen.

Page 34, paragraph # 93:

In this case, the data reference is performed on only signals of one system such as G or Y on which energy is liable to be concentrated and in which image deterioration is more apparent, the

sampling clock phase is optimized and the sampling is applied to the signals of the other systems at the same phase as G or Y.

Page 43, insert BEFORE paragraph # 117:

-- In the above embodiments, the video signals are output as analog signals to be displayed on a CRT display. However, some video signal generators output the video signals as digital signals to be displayed on a liquid crystal display (LCD) or a plasma display.

The A/D converters of the above embodiments perform two functions. The first function is to convert an analog signal value to the corresponding discrete digital data. The second function is to determine the representative value within a sampling period. The timing of the determination is controlled by the sampling clock which is provided as an input signal. As described above, the phase of the sampling clock has to be properly adjusted according to the phase of picture element data.

When the video signal generators, such as personal computer and engineering workstation, output the digital video signals, it is unnecessary for the video signal processing device to convert the input signal to the discrete digital data. In other words, only the second function of the A/D converter is necessary for the video signal processing device which is to be connected to the video signal generator which outputs the digital video signal.

In this case, the video signal generator holds the digital video signal data corresponding to a picture element to be displayed on a display screen during the time corresponding to the picture element period on the display screen. The video signal processing device has to sample the output digital video signal according to the phase of the picture element data to receive the correct data. The adjustment of the phase of the sampling clocks can be performed in the same way as the above embodiments.

REMARKS

It is believed that the application is now in condition for examination on the merits, which is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and title and claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made."**

The Examiner is invited to call the undersigned at (202) 220-4200 to discuss any information concerning this application.

The Office is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: February 11, 2002

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As described above, the sampling clocks are controlled to be synchronized with the horizontal synchronizing signals by the PLL. However, [actually] actuality, the phase of the sampling clocks generated on the basis of the synchronizing signals is not always synchronized in phase with the dot phase due to [a] the processing delay of a synchronizing separating circuit for separating the horizontal synchronizing signals from the video signals (when the synchronizing signals are transmitted while superposed on the video signals), the difference in processing delay between the horizontal synchronizing signals and the video signals which are normally processed in a different system, or the variance between the length of a transmission cable for transmitting the horizontal synchronizing signals and the length of a transmission cable for transmitting the video signals (when the synchronizing signals are transmitted independently from the video signals). Therefore, in this case, the phase of the sampling clocks or the synchronizing signals is required to be delayed through a delay line, thereby adjusting the sampling clock phase.

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In order to attain the above object according to the present invention, the video signal processing device [according to the present invention] in which video signals representing an image are converted to multi-valued digital data representing picture elements each contained in the image at a timing based on sampling clocks, includes conversion means for successively sampling the video signals at the timing based on the sampling clocks to convert the video signals to the multi- valued digital data, classification means for successively classifying the converted multi-valued digital data into a low-level picture-element data group having values contained in a first value range and a high-

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Fig. 5 [is] contains graphs showing the relationship between the sampling clock phase and the occurrence frequency of (a) the data of the difference AT between the average values of white picture element data and black picture element data, and (b) the total variance VT of the variance of the white picture element data and the variance of the black picture element data;

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[Now, from the] The video signal generator 19 [is input] inputs, as [input] video [signals] signals, a test pattern which comprises signals having two gradation levels, for example, a black signal (0% brightness) having a level lower than a predetermined level and a white signal (100% brightness) having a level higher than the predetermined level and in which variations from black to white and from white to black occur relatively frequently.

Page 21, paragraph # 62:

Upon an instruction [of the adjustment of] to adjust the sampling clock phase from the controller 21 through the communication terminal 16 after [it is started] the video signal generator 19 starts to input the input video signals VI of the black and white pattern as shown in Fig. 4A [from the video signal generator 19], the MPU 9 first reads data from the memory 6 to calculate the average difference AT and the total variance VT (first). Thereafter, the phase of the sampling clocks generated in the write-in control circuit 5 on the basis of the control signal CKPH from the MPU 9 is varied in a specific direction (for example, a plus direction). In this state, the data which are sampled and digitally converted in the A/D converter 4 are read out from the memory 6 again to calculate the average difference AT and the total variance VT (second).

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